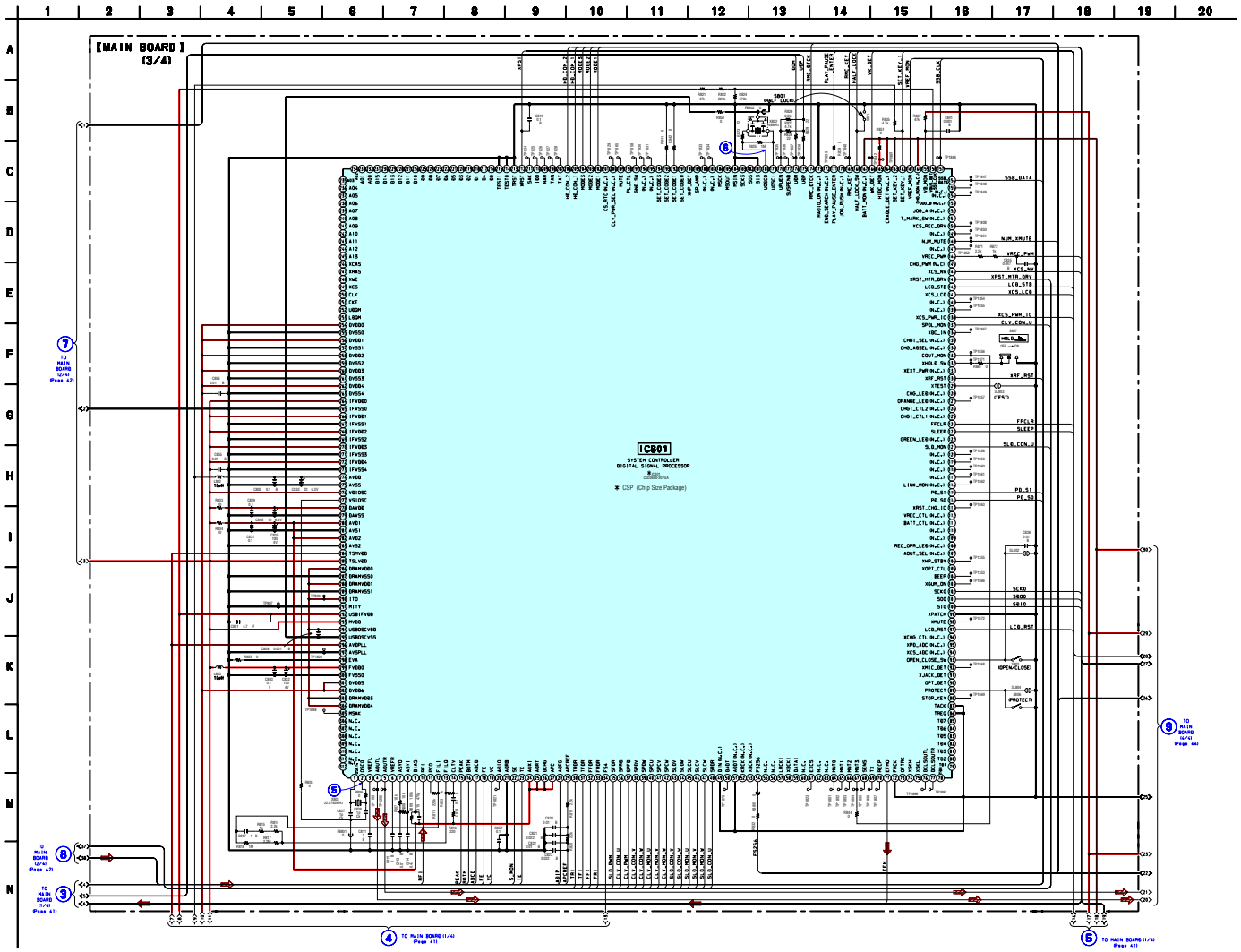
6-6. SCHEMATIC DIAGRAM – MAIN BOARD (3/4) – • See page 49 for IC PIN FUNCTION DESCRIPTION. • See page 37 for Waveforms.



• IC PIN FUNCTION DESCRIPTION

• IC801 CXD2680-207GA (SYSTEM CONTROLLER, DIGITAL SIGNAL PROCESSOR)

Pin No.	Pin Name	I/O	Description
1	OSCI	I	Resonator connection terminal for the system clock (22.5792MHz)
2	OSCO	O	Resonator connection terminal for the system clock (22.5792MHz)
3	VREFL	O	Reference voltage terminal connected to the capacitor (for the built-in D/A converter L-CH)
4	AOUTL	O	Built-in D/A converter L-CH signal output
5	AOUTR	O	Built-in D/A converter R-CH signal output
6	VREFR	O	Reference voltage terminal connected to the capacitor (for the built-in D/A converter R-CH)
7	ASYO	O	Playback EFM duplex signal output
8	ASYI	I	Playback EFM comparator slice level input
9	BIAS	I	Bias current input terminal for the playback EFM comparator
10	RFI	I	Playback EFM RF signal input from the RF amplifier
11	PCO	O	Phase comparison output terminal for the playback EFM system master PLL
12	FILI	I	Filter input terminal for the playback EFM system master PLL
13	FILO	O	Filter output terminal for the playback EFM system master PLL
14	CLTV	I	Internal VCO control voltage input terminal for the playback EFM system master PLL
15	PEAK	I	Peak hold signal input of the light amount signal (RF/ABCD) from the RF amplifier
16	BOTM	I	Bottom hold signal input of the light amount signal (RF/ABCD) from the RF amplifier
17	ABCD	I	Light amount signal (ABCD) input from the RF amplifier
18	FE	I	Focus error signal input from the RF amplifier
19	VC	I	Middle point voltage input from the RF amplifier
20	ADIO	O	Monitor output terminal of A/D converter input signal Not used (open)
21	ADRB	I	The lower limit voltage of A/D converter input terminal (connected to the ground)
22	SE	I	Sled error signal input from the RF amplifier
23	TE	I	Tracking error signal input from the RF amplifier
24	AUX1	I	Auxiliary A/D input (fixed at "H" in this set)
25	ADRT	I	The upper limit voltage of A/D converter input terminal (fixed at "H" in this set)
26	DCHG	I	Connecting terminal with the analog power supply of low impedance (fixed at "H" in this set)
27	APC	I	Error signal input for the laser automatic power control (fixed at "H" in this set)
28	ADFG	I	ADIP duplex FM signal (22.05±1kHz) input from the RF amplifier
29	APCREF	O	Reference PWM signal output for the laser automatic power control to the RF amplifier
30	TRDR	O	Tracking servo drive PWM signal output (–) to the coil driver
31	TFDR	O	Tracking servo drive PWM signal output (+) to the coil driver
32	FFDR	O	Focus servo drive PWM signal output (+) to the coil driver
33	FRDR	O	Focus servo drive PWM signal output (–) to the coil driver
34	FS4	O	176.4kHz clock signal output
35	SFDR	O	Sled servo drive PWM signal output to the motor driver
36	SPRD	O	Spindle motor drive control signal output (U) to the motor driver
37	SPFD	O	Spindle servo drive PWM signal output to the motor driver
38	SPDV	O	Spindle motor drive control signal output (V) to the motor driver
39	SPDW	O	Spindle motor drive control signal output (W) to the motor driver
40	SPCU	I	Spindle motor drive comparison signal input (U) from the motor driver
41	SPCV	I	Spindle motor drive comparison signal input (V) from the motor driver
42	SPCW	I	Spindle motor drive comparison signal input (W) from the motor driver
43	SLDV	O	Sled motor drive control signal output (V) to the motor driver
44	SLDW	O	Sled motor drive control signal output (W) to the motor driver
45	SLCU	I	Sled motor drive comparison signal input (U) from the motor driver
46	SLCV	I	Sled motor drive comparison signal input (V) from the motor driver
47	SLCW	I	Sled motor drive comparison signal input (W) from the motor driver
48	SRDR	O	Sled motor drive control signal output (U) to the motor driver
49	DIN	I	Digital audio signal input (fixed at "L" in this set)
50	DADT	O	Audio data output terminal Not used (open)

Pin No.	Pin Name	I/O	Description
51	ADDT	I	Data input from the external A/D converter (fixed at "L" in this set)
52	KRCK	O	L/R sampling clock (44.1KHz) output to the external A/D converter Not used (open)
53	XBCK	O	Bit clock (2.8224MHz) output to the external A/D converter Not used (open)
54	FS256	O	11.2896MHz clock output
55	NC	O	Filter cutoff control signal output Not used (open)
56	NC	I	Clock input from the external VCO Not used (open)
57	LRCKI	I	Input terminal for the PCM data I/F/ ATRAC data I/F Not used (open)
58	XBCKI	I	Input terminal for the PCM data I/F/ ATRAC data I/F Not used (open)
59	DATAI	I	Input terminal for the PCM data I/F/ ATRAC data I/F Not used (open)
60	NC	—	Not used (open)
61	EXCS	O	Chip select signal output teminal for the external SDRAM Not used (open)
62, 63	NC	—	Not used (open)
64 to 66	MNT0 to 2	O	DSP monitor (0) to (2) output terminal Not used (open)
67	MNT3	O	DSP monitor (3) output terminal
68	SENS	O	DSP internal status (DSP SENS monitor) signal output terminal Not used (open)
69	TX	O	Record data output enable signal output Not used (open)
70	RECP	O	Laser power changeover signal output Not used (open)
71	EFMO	O	EFM encode data output for the record to the REC driver
72	FMCK	I	FMCK signal input Not used (connected to the ground)
73	OFTRK	I/O	Tracking signal input/output Not used (open)
74	XSKH	O	L circuit signal output Not used (open)
75	XSKL	O	K-SHOCK circuit signal output Not used (open)
76	DCLSOUTL	O	PWM modulator signal output for the D class headphone amplifier Not used (open)
77	DCLSOUTR	O	PWM modulator signal output for the D class headphone amplifier Not used (open)
78 to 85	TD0 to 7	—	TigerI/F data 0 to 7 terminal Not used (open)
86	TREQ	—	TigerI/F REQUEST terminal Not used (connected to the ground)
87	TACK	—	TigerI/F ACK terminal Not used (connected to the ground)
88	STOP_KEY	I	Stop key detection input terminal from the switch & liquid crystal display module Not used (open)
89	PROTECT	I	Detection signal input terminal of the record check claw from the protect detection switch "H": protect
90	OPT_DET	I	DIN plug detection signal input "H": DIN plug detect Not used (open)
91	XJACK_DET	I	LINE IN plug detection signal input "L": LINE or OPT plug detect Not used (open)
92	XMIC_DET	I	Microphone plug detection signal input "L": microphone plug detect Not used (open)
93	OPEN_CLOSE_SW	I	Open/close detection switch of the upper panel input terminal "L": when upper panel close
94	XCS_ADC	O	Chip select signal output to the A/D converter Not used (open)
95	XPD_ADC	O	Power supply control signal output to the A/D converter Not used (open)
96	XCHG_CTL	O	Charge ON/OFF control signal output Not used (open)
97	LCD_RST	O	Reset control signal output to the liquid crystal display module
98	XMUTE	O	Analog muting control signal output to the headphone amplifier "L": muting ON Not used (open)
99	XPATCH	I	Patch function detection terminal "L": patch function (fixed at "L" in this set)
100	SI0	I	Serial data input from the nonvolatile memory
101	SO0	O	Serial data output to the nonvolatile memory, liquid crystal display module and power control
102	SCK0	O	Serial clock output to the nonvolatile memory, liquid crystal display module and power control
103	XGUM_ON	I	Rechargeable battery detection switch input terminal "L": rechargeable battery in detect Not used (open)
104	BEEP	O	Beep sound control signal output to the headphone amplifier Not used (open)
105	XOPT_CTL	O	Power supply ON/OFF control signal output for the DIN PD drive Not used (open)
106	XHP_STBY	O	Power supply control signal output to the headphone amplifier Not used (open)
107	AOUT_SEL	O	HP/LINE changeover signal output to the headphone amplifier Not used (open)
108	REC_OPR_LED	O	LED ON/OFF control signal output for the REC display Not used (open)
109	NC	O	Power supply control signal output for the OP modulation Not used (open)
110	NC	O	Power supply control signal output for the OP laser Not used (open)

Pin No.	Pin Name	I/O	Description
111	BATT_CTL	O	Control signal output for the voltage step up circuit in the external battery case Not used (open)
112	VREC_CTL	O	VREC voltage control signal output Not used (open)
113	XRST_CHG_IC	O	Reset signal output to the battery charge control IC Not used (open)
114, 115	PD_S0, 1	O	PD IC mode changeover signal output to the optical pick up
116	LINK_MON	O	Linking area monitor signal output Not used (open)
117	NC	O	Plunger control signal output Not used (open)
118	NC	O	Ground changeover switch control signal output Not used (open)
119, 120	NC	O	Not used (open)
121	SLD_MON	I	Sled servo monitor signal input
122	GREEN_LED	O	Not used (open)
123	SLEEP	O	System sleep control signal output to the power control
124	FFCLR	O	Input latch output for the start switching to the power control
125	CHGI_CTL1	O	Charge current limit ON/OFF control signal output at the time of adaptor use Not used (open)
126	CHGI_CTL2	O	Charge current limit value changeover control signal output at the time of adaptor use Not used (open)
127	ORANGE_LED	O	Orange LED ON/OFF control signal output Not used (open)
128	CHG_LED	O	LED ON/OFF control signal output for CHG (charge display) Not used (open)
129	XTEST	I	Terminal for the test mode setting (normally open) “L”: test mode
130	XRF_RST	O	Reset control signal output to the RF amplifier “L”: reset
131	XEXT_PWR	I	External power supply (AC adaptor/charging stand) detection signal input Not used (open)
132	XHOLD_SW	I	HOLD switch input terminal “L”: hold ON
133	COUT_MON	I	Traverse count measurement monitor input
134	CHG_ADSEL	O	A/D terminal of the battery charge contro IC output selection signal output Not used (open)
135	CHGI_SEL	O	Charge/discharge changeover control signal output for the current sense amplifier Not used (open)
136	XDC_IN	I	DC plug detection signal input Not used (open)
137	SPDL_MON	I	Spindle servo monitor signal input
138	XCS_PWR_IC	O	Chip select signal output to the power control
139, 140	NC	O	Control signal output for the D class headphone amplifier Not used (open)
141	XCS_LCD	O	Chip select signal output to the liquid crystal display module
142	LCD_STB	O	Strobe signal output to the liquid crystal display module
143	XRST_MTR_DRV	O	Reset control signal output to the motor driver “L”: reset
144	XCS_NV	O	Chip select signal output to the nonvolatile memory
145	CHG_PWM	O	Output voltage control signal output to the battery charge control Not used (open)
146	VREC_PWM	O	PWM signal output for the power supply voltage control to the REC driver
147	NC	O	PWM signal output for the laser power supply voltage control to the power control Not used (open)
148	NJM_XMUTE	O	Muting control signal to the headphone amplifier (NJM type made by JRC)
149	NC	O	Power supply control signal output for the D class headphone amplifier Not used (open)
150	XCS_REC_DRV	O	Chip select signal output to the REC driver Not used (open)
151	T_MARK _SW	I	T MARK (track mark) switch input terminal “L”: track mark detection Not used (open)
152	JOG_A	I	Jog dial pulse input from the switch & liquid crystal display module Not used (open)
153	JOG_B	I	Jog dial pulse input from the switch & liquid crystal display module Not used (open)
154, 155	NC	O	Not used (open)
156	SSB_DATA	I/O	SSB data input/output with the RF amplifier
157	SSB_CLK	O	SSB clock output to the RF amplifier
158	VBUS_DET	I	USB power supply voltage detection terminal
159	VB_MON	I	Voltage monitor input terminal (A/D input) of the UNREG power supply
160	CHG_MON	I	Not used (fixed at “H”)
161	VREF_MON	I	Reference voltage monitor input (A/D input) from the RF amplifier
162	SET_KEY_1	I	Key input (A/D input) from the switch & liquid crystal display module
163	SET_KEY_2	I	Key input (A/D input) from the switch & liquid crystal display module Not used (fixed at “H”)
164	CRADLE_DET	I	USB cradle or battery case detection signal input Not used (fixed at “H”)

Pin No.	Pin Name	I/O	Description
165	HIDC_MON	I	HIGH DC voltage monitor input (A/D input) Not used (fixed at “H”)
166	WK_DET	I	Set key WAKE detection signal input
167	BATT_MON	I	External battery voltage monitor input Not used (fixed at “H”)
168	HALF_LOCK_SW	I	Open button detection switch input (A/D input) “L” : the open button is pressed
16 9	RMC_KEY	I	Key input (A/D input) from the remote commander
170	JOG_PUSH	I	Jog dial push detection signal input Not used (open)
171	PLAY_PAUSE_ENTER	I	PLAY_PAUSE_ENTER key input (A/D input)
172	END_SEARCH	I	END SEARCH key input (A/D input) Not used (open)
173	RADIO_ON	I	RADIO ON detection signal input Not used (connected to the ground)
174	RMC_DTCK	I/O	TSB master data clock input/output or SSB data input/output
175	UDP	I/O	USB data (+) input terminal
176	UDM	I/O	USB data (-) input terminal
177	SUSPEND	O	USB suspend signal output Not used (open)
178	UPUEN	O	USB pull-up resistor connection control output terminal
179	UOSCI	I	Resonator (48MHz) connection terminal for the USB oscillation circuit
180	UOSCO	O	Resonator (48MHz) connection terminal for the USB oscillation circuit
181	SI3	I	Not used (connected to the ground)
182	SO3	O	Not used (open)
183	SCK3	I/O	Not used (open)
184	MSIN	I	Not used (connected to the ground)
185	MSOUT	O	Not used (open)
186	MSCK	I/O	Not used (open)
187, 188	NC	O	Not used (open)
189	SP_AMP	O	Built-in speaker control signal output “H”: activate Not used (open)
190	XHP_DET	I	Headphone jack detection signal input Not used (open)
191	SET_CODE0	I	Input terminal for the set (open in this set)
192	SET_CODE1	I	Input terminal for the set (fixed at “L” in this set)
193	SET_CODE2	I	Input terminal for the set (fixed at “L” in this set)
194	SET_CODE3	I	Input terminal for the set (open in this set)
195, 196	NC	O	Not used (open)
197	GND_SW	I	Not used (open)
198	PL_CTL	O	Not used (open)
199	MUTE	O	Analog muting control signal output to the headphone amplifier “H”: muting ON Not used (open)
200	CLV_PWR_SEL	O	CLV motor power supply selection control signal output Not used (open)
201	CS_RTC	O	Chip select signal output to the real time clock Not used (open)
202 to 204	MODE1 to 3	O	Power supply control signal output for the over write head to the REC driver
205, 206	HD_CON_1, 2	O	Over write head control signal output to the REC driver
207	TAT	I	Not used (open)
208	TAN	I	Not used (open)
209	NAR	I	Not used (open)
210	IDO	I	Not used (open)
211	SAK	O	Not used (open)
212	XRST	I	System reset signal input from the power control “L”: reset
213	TRST	I	Terminal for the test mode setting (normally fixed at “L”)
214, 215	TEST0, 1	I	Input terminal for the main test (normally fixed at “L”)
216 to 231	D0 to 15	—	DRAM data0 to 15 terminal Not used (open)
232 to 245	A00 to 13	—	DRAM address0 to 13 terminal Not used (open)
246	XCAS	—	DRAM CAS terminal Not used (open)
247	XRAS	—	DRAM RAS terminal Not used (open)
248	XWE	—	DRAM write enable terminal Not used (open)

Pin No.	Pin Name	I/O	Description
249	XCS	—	DRAM chip select terminal Not used (open)
250	CLK	—	DRAM clock terminal Not used (open)
251	CKE	—	DRAM clock enable terminal Not used (open)
252	UDQM	—	DRAM byte mask terminal Not used (open)
253	LDQM	—	DRAM byte mask terminal Not used (open)
254	DVDD0	—	Power supply terminal
255	DVSS0	—	Ground terminal
256	DVDD1	—	Power supply terminal
257	DVSS1	—	Ground terminal
258	DVDD2	—	Power supply terminal
259	DVSS2	—	Ground terminal
260	DVDD3	—	Power supply terminal
261	DVSS3	—	Ground terminal
262	DVDD4	—	Power supply terminal
263	DVSS4	—	Ground terminal
264	IFVDD0	—	Power supply terminal (for the microcomputer I/F block)
265	IFVSS0	—	Ground terminal (for the microcomputer I/F block)
266	IFVDD1	—	Power supply terminal (for the microcomputer I/F block)
267	IFVSS1	—	Ground terminal (for the microcomputer I/F block)
268	IFVDD2	—	Power supply terminal (for the microcomputer I/F block)
269	IFVSS2	—	Ground terminal (for the microcomputer I/F block)
270	IFVDD3	—	Power supply terminal (for the microcomputer I/F block)
271	IFVSS3	—	Ground terminal (for the microcomputer I/F block)
272	IFVDD4	—	Power supply terminal (for the microcomputer I/F block)
273	IFVSS4	—	Ground terminal (for the microcomputer I/F block)
274	AVDD	—	Power supply terminal (for the microcomputer analog)
275	AVSS	—	Ground terminal (for the microcomputer analog)
276	VDIOSC	—	Power supply terminal (for the OSC cell)
277	VSIOSC	—	Ground terminal (for the OSC cell)
278	DAVDD	—	Power supply terminal (for the built-in D/A converter)
279	DAVSS	—	Ground terminal (for the built-in D/A converter)
280	AVD1	—	Power supply terminal (for the DSP asymmetry system analog)
281	AVS1	—	Ground terminal (for the DSP asymmetry system analog)
282	AVD2	—	Power supply terminal (for the DSP servo system analog)
283	AVS2	—	Ground terminal (for the DSP servo system analog)
284	TSMVDD	—	Power supply terminal (for the TSB master communication)
285	TSLVDD	—	Power supply terminal (for the TSB slave I/F)
286	DRAMVDD0	—	Power supply terminal (for DRAM)
287	DRAMVSS0	—	Ground terminal (for DRAM)
288	DRAMVDD1	—	Power supply terminal (for DRAM)
289	DRAMVSS1	—	Ground terminal (for DRAM)
290	ITO	—	Power supply terminal (for writing the flash memory)
291	MITY	—	Ground terminal (for writing the flash memory)
292	USBIFVDD	—	Power supply terminal (for USB I/F)
293	MVDD	—	Power supply terminal (for the microcomputer I/F block)
294	USBOSCVDD	—	Power supply terminal (for the USB oscillation circuit)
295	USBOSCVSS	—	Ground terminal (for the USB oscillation circuit)
296	AVDPLL	—	Power supply terminal (for PLL)
297	AVSPLL	—	Ground terminal (for PLL)
298	EVA	I	EVA terminal (fixed at “L” in this set)

Pin No.	Pin Name	I/O	Description
299	FVDD0	—	Power supply terminal (for the built-in flash memory)
300	FVSS0	—	Ground terminal (for the built-in flash memory)
301, 302	DVDD5, 6	—	Power supply terminal
303, 304	DRAMVDD3, 4	—	Power supply terminal (for DRAM)
305	MSAK	—	Not used (open)
306 to 312	NC	—	Not used (open)