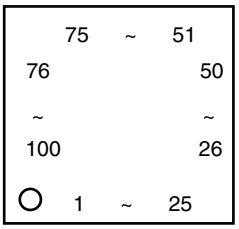
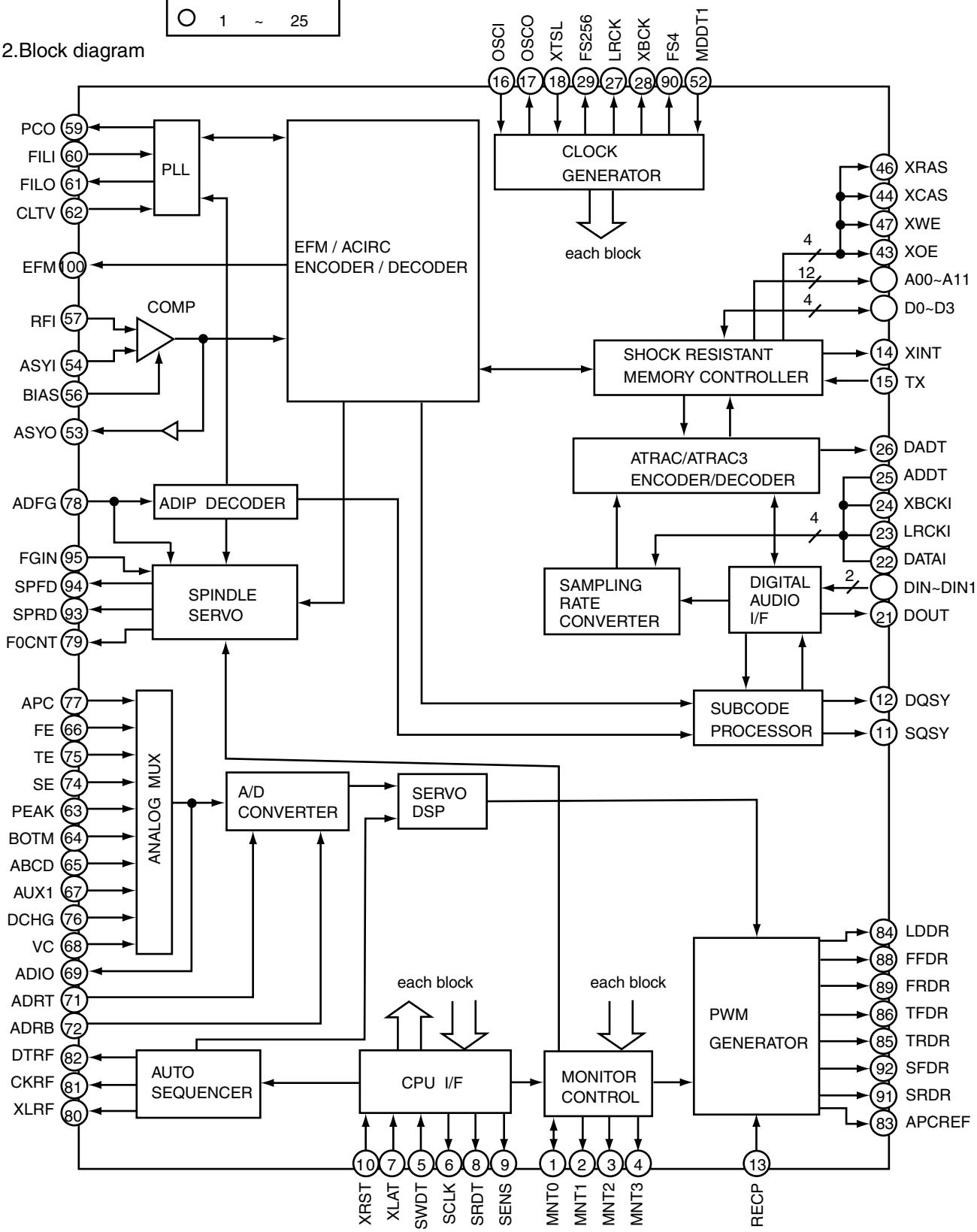
■ CXD2662R (IC350) : DSP

1.Terminal layout



2.Block diagram



3.Pin function

Pin No.	Symbol	I/O	Function
1	MNT0	I/O	Monitor output.
2	MNT1	O	Monitor output.
3	MNT2	O	Monitor output.
4	MNT3	O	Monitor output.
5	SWDT	I	Data input for microcomputer serial interface.
6	SCLK	I	Shift clook input for microcomputer serial interface.
7	XLAT	I	Latch input for microcomputer serial interface.Latched at the falling edge.
8	SRDT	O	Data output for microcomputer serial interface.
9	SENS	O	Outputs the internal status corresponding to the microcomputer serial interface address.
10	XRST	I	Reset input. Low : reset
11	SQSY	O	Disc subcode Q sync / ADIP sync output.
12	DQSY	O	Subcode Q sync output in U-bit CD or MD format when the Digital In source is CD or MD.
13	RECP	I	Laser power switching input. High : recording power ; low ; playback power
14	XINT	O	Interruption request output. Low when the interruption status occurs.
15	TX	I	Enable signal input for recoding data output. High : enabled
16	OSCI	I	Crystal oscillation circuit input.
17	OSCO	O	Crystal oscillation circuit output. (inverted output of the OSCI pin)
18	XTSL	I	OSCI input frequency switching. XTSL1(command) = low and XTSL = high : 512Fs (22.5792MHz) XTSL1(command) = low and XTSL = low : 1024Fs (45.1584MHz) XTSL1(command) = high : 2048Fs (90.3168MHz)
19	DIN0	I	Digital audio interface signal input 1.
20	DIN1	I	Digital audio interface signal input 2.
21	DOUT	O	Digital audio interface signal output.
22	DATAI	I	Test pin. Connect to GND.
23	LRCKI	I	Test pin. Connect to GND.
24	XBCKI	I	Test pin. Connect to GND.
25	ADDT	I	Data input from A / D converter.
26	DADT	O	REC monitor output / decoded audio data output.
27	LRCK	O	LA clock (44.1kHz) output to the external audio block.
28	XBCK	O	Bit clock (2.8224kHz) output to the external audio block.
29	FS256	O	256Fs output.
30	DVDD	-	Digital power supply.
31	A03	O	External DRAM address output.
32	A02	O	External DRAM address output.
33	A01	O	External DRAM address output.
34	A00	O	External DRAM address output.
35	A10	O	External DRAM address output.
36	A04	O	External DRAM address output.
37	A05	O	External DRAM address output.
38	A06	O	External DRAM address output.
39	A07	O	External DRAM address output.
40	A08	O	External DRAM address output.
41	A11	O	External DRAM address output.
42	DVSS	-	Digital ground.
43	XOE	O	External DRAM output enable.

Pin No.	Symbol	I/O	Function
44	XCAS	O	External DRAM CAS output.
45	A09	O	External DRAM address output.
46	XRAS	O	External DRAM RAS output.
47	XWE	O	External DRAM write enable.
48	D1	I/O	External DRAM data bus.
49	D0	I/O	External DRAM data bus.
50	D2	I/O	External DRAM data bus.
51	D3	I/O	External DRAM data bus.
52	MDDTI	I	MD-DATA mode 1 switching input. (Low : normal mode ; high : MD-DATA mode 1)
53	ASYO	O	Playback EFM full-swing input. (Low : vss ; high : Vdd)
54	ASYI	I	Playback EFM comparator slice voltage input.
55	AVDD	-	Analog power supply.
56	BIAS	I	Playback EFM comparator bias current input.
57	RFI	I	Playback EFM RE signal input.
58	AVSS	-	Analog ground.
59	PCO	O	Phase comparison output for master PLL of playback digital PLL and recording EFM PLL.
60	FILI	I	Filter input for master PLL of playback digital PLL and recording EFM PLL.
61	FILO	O	Filter output for master PLL of playback digital PLL and recording EFM PLL.
62	CLTV	I	Internal VCO control voltage input for master PLL of playback digital EFM PLL and recording EFM PLL.
63	PEAK	I	Peak hold signal input for quantity of light.
64	BOTM	I	Bottom hold signal input for quantity of light.
65	ABCD	I	Signal input for quantity of light.
66	FE	I	Focus error signal input.
67	AUXI	I	Auxillary input 1.
68	VC	I	Center voltage input.
69	ADIO	I	Monitor output for A / D converter input signal.
70	AVDD	-	Analog power supply.
71	ADRT	I	Voltage input for the upper limit of the A / D converter operating range.
72	ADRB	I	Voltage input for the lower limit of the A / D converter operating range.
73	AVSS	-	Analog ground.
74	SE	I	Sled error signal input.
75	TE	I	Tracking error signal input.
76	DCHG	I	Connect to he low-inpedance power supply.
77	APC	I	Error signal input for laser digital APC.
78	ADFG	I	ADIP binary FM signal (22.05 ± 1kHz) input.
79	F0CNT	O	CXA2523 current source setting output.
80	XLRF	O	CXA2523 control latch output. Latched at the falling edge.
81	CKRF	O	CXA2523 control shift clock output.
82	DTRF	O	CXA2523 control data output.
83	APCREF	O	Reference PWM output for laser APC.
84	LDDR	O	PWM output for laser digital APC.
85	TRDR	O	Tracking servo drive PWM output. (–)
86	TFDR	O	Tracking servo drive PWM output. (+)
87	DVDD	-	Digital power supply.
88	FFDR	O	Focus servo drive PWM output. (+)
89	FRDR	O	Focus servo drive PWM output. (–)
90	FS4	O	4Fs output. (176.4kHz)

Pin No.	Symbol	I/O	Function
91	SRDR	O	Sled servo drive PWM output. (−)
92	SFDR	O	Sled servo drive PWM output. (+)
93	SPRD	O	Spindle servo drive output. (PWM (−) or polarity)
94	SPFD	O	Spindle servo drive output. (PWM (+) or PWM absolute value)
95	FGIN	I	Spindle CAV servo FG input.
96	TEST1	I	Test pin. Connect to GND.
97	TEST2	I	Test pin. Connect to GND.
98	TEST3	I	Test pin. Connect to GND.
99	DVSS	-	Digital ground.
100	EFMO	O	Low when playback ; EFM (encoded data) output when recording.