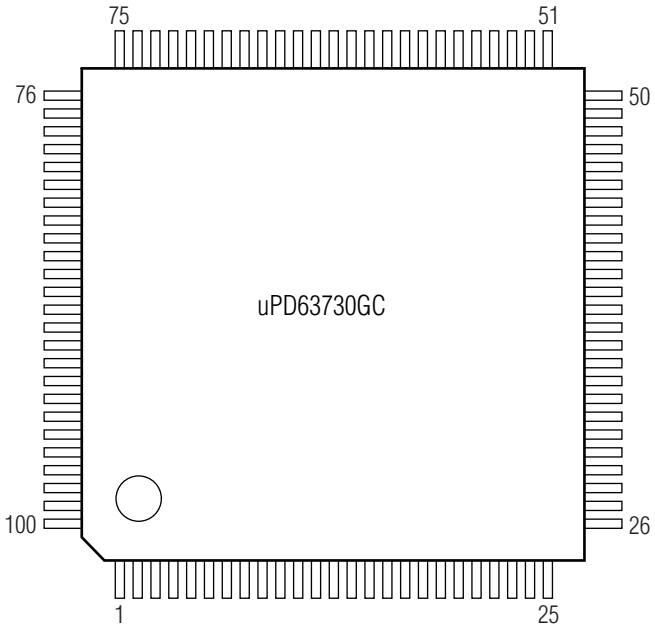
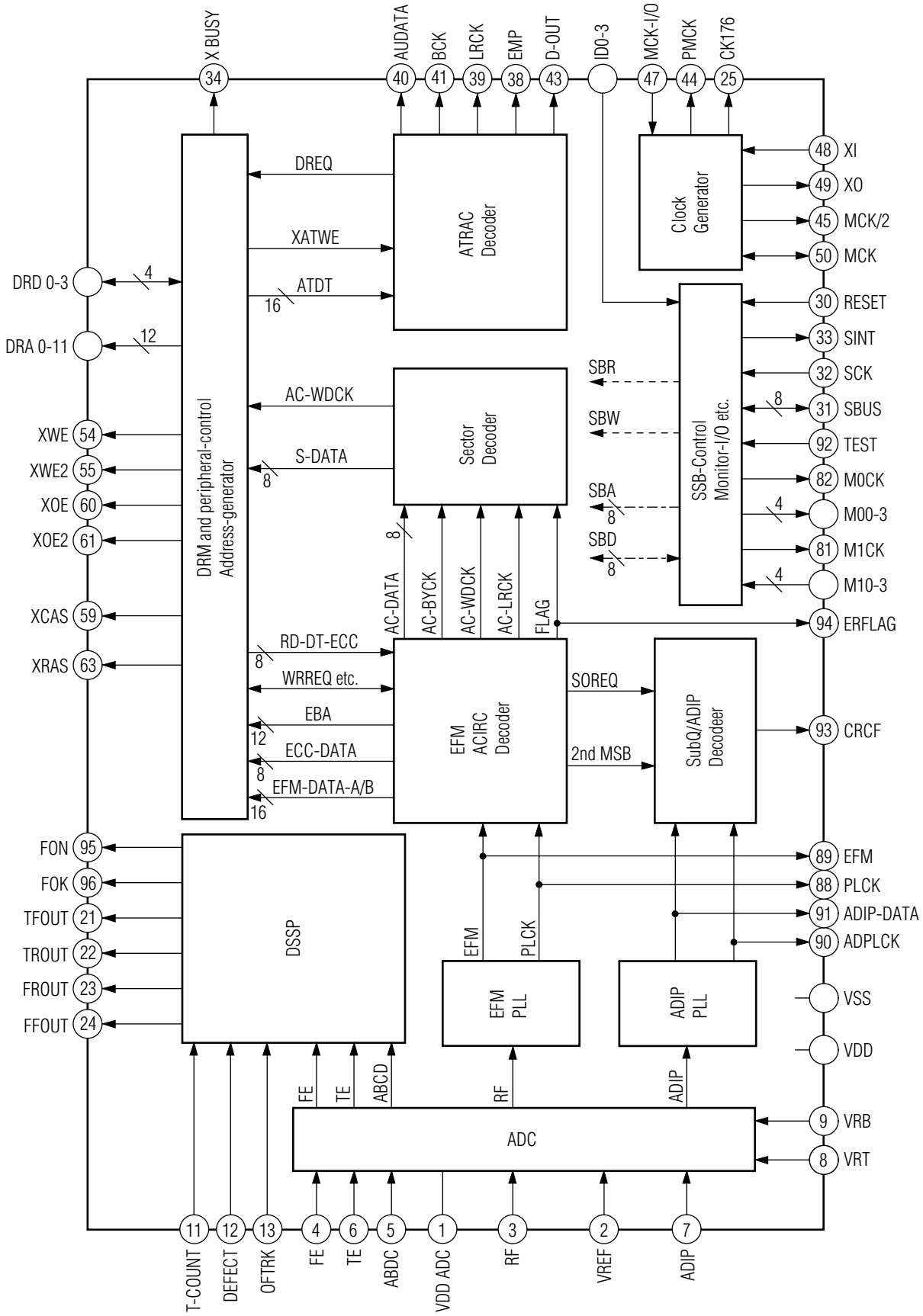
10-2. DSP/Digital Servo µPD63730GC

DSP/digital servo for MD playback

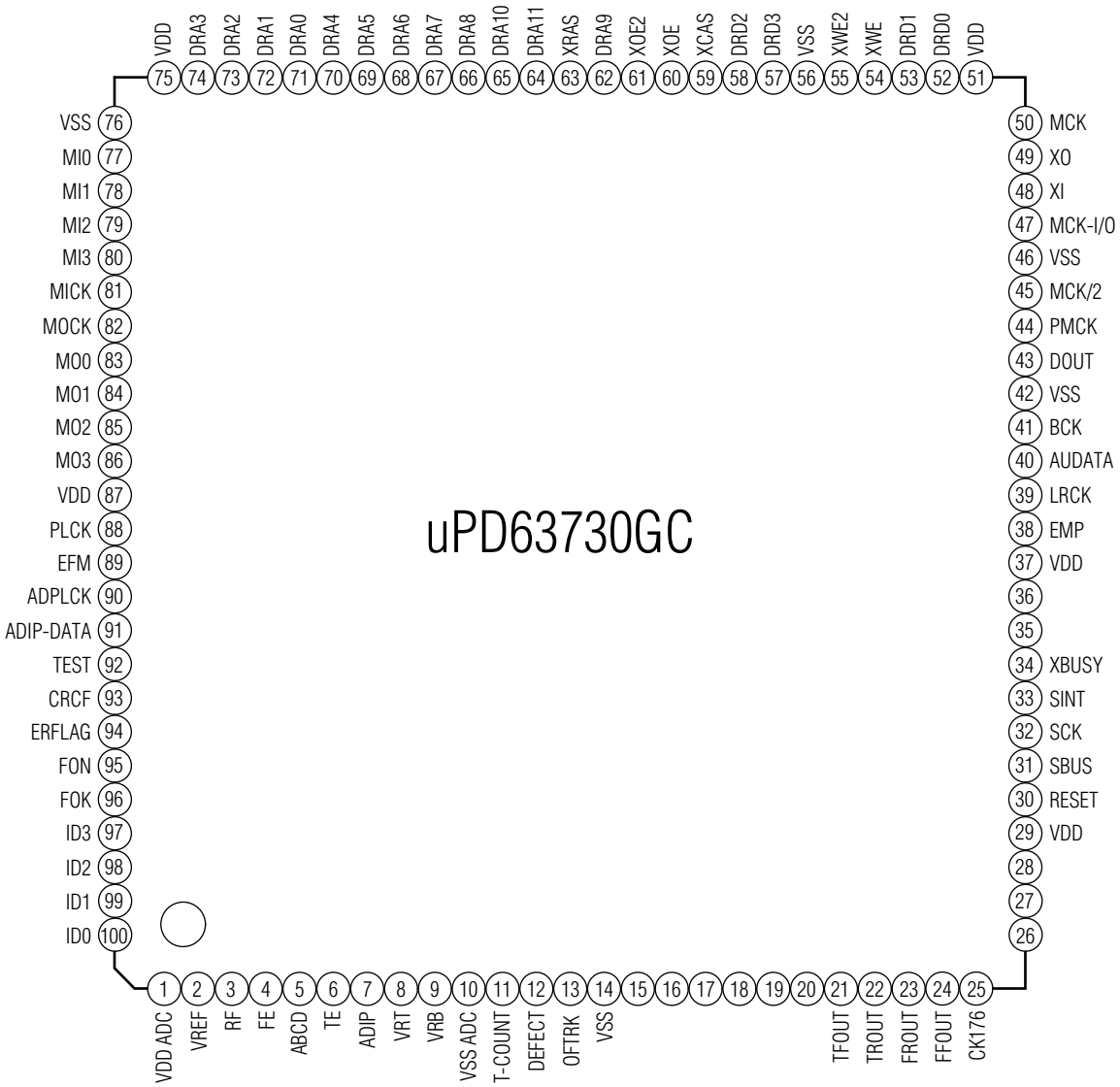
- Built-in ATRAC decoder for playback
- Digital servo, EFM decoder, and ACIRC decoder functions



Internal Block Diagram



Pin Configuration



Pin Function

Pin No.	Symbol	I/O	Function
1	VDD ADC	—	Power supply for ADC block
2	VREF	I	Reference voltage input
3	RF	I	RF signal input
4	FE	I	Focus error input
5	ABCD	I	ABCD (all quantity of light) signal input
6	TE	I	Tracking error input
7	ADIP	I	ADIP signal input
8	VRT	I	ADC high potential reference voltage for RF
9	VRB	I	ADC low potential reference voltage for other than RF
10	VSS ADC	—	Ground for ADC block
11	T-COUNT	I	Tracking count signal input
12	DEFECT	I	Defect signal input
13	OFTRK	I	Off track signal input
14	VSS	—	Ground
15			
16			
17			
18			
19			
20			
21	TFOUT	O	Tracking servo output (1)
22	TROUT	O	Tracking servo output (2)
23	FROUT	O	Focus servo output (1)
24	FFOUT	O	Focus servo output (2)
25	CK176	O	176.4 kHz (4 fs) output
26			
27			
28			
29	VDD	—	Power supply
30	RESET	I	Reset input. Reset when “L”.
31	SBUS	I/O	SBUS interface input/output
32	SCK	I	SBUS clock input
33	SINT	O	Interrupt signal output
34	XBUSY	O	DRAM access status
35			
36			
37	VDD	—	Power supply
38	EMP	O	Emphasis output for DAC. ON when ‘H”.
39	LRCK	O	L/R clock output
40	AUDATA	O	Audio data output
41	BCK	O	Bit clock output
42	VSS	—	Ground
43	DOUT	O	Digital output
44	PMCK	O	1/4 divided output of MCK
45	MCK/2	O	1/2 divided output of MCK
46	VSS	—	Ground
47	MCK I/O	I	Input/output direction switching of MCK. “L”:output, “H”:input.
48	XI	I	Crystal oscillation input (384 fs=16.93 MHz)
49	XO	O	Crystal oscillation output
50	MCK	I/O	Master clock input/output

Pin No.	Symbol	I/O	Function
51	VDD	—	Power supply
52	DRD0	I/O	DRAM data input/output
53	DRD1	I/O	DRAM data input/output
54	XWE	O	DRAM write enable output
55	XWE2	O	DRAM write enable output
56	VSS	—	Ground
57	DRD3	I/O	DRAM data input/output
58	DRD2	I/O	DRAM data input/output
59	XCAS	O	DRAM-CAS output
60	XOE	O	DRAM output enable output
61	XOE2	O	DRAM output enable output
62	DRA9	O	DRAM address output
63	XRAS	O	DRAM-RAS output
64	DRA11	O	DRAM address output
65	DRA10	O	DRAM address output
66	DRA8	O	DRAM address output
67	DRA7	O	DRAM address output
68	DRA6	O	DRAM address output
69	DRA5	O	DRAM address output
70	DRA4	O	DRAM address output
71	DRA0	O	DRAM address output
72	DRA1	O	DRAM address output
73	DRA2	O	DRAM address output
74	DRA3	O	DRAM address output
75	VDD	—	Power supply
76	VSS	—	Ground
77	M10	I/O	Monitor input
78	M11	I/O	Monitor input
79	M12	I/O	Monitor input
80	M13	I/O	Monitor input
81	MICK	O	Monitor in clock
82	MOCK	O	Monitor out clock
83	M00	O	Monitor output
84	M01	O	Monitor output
85	M02	O	Monitor output
86	M03	O	Monitor output
87	VDD	—	Power supply
88	PLCK	I/O	PLL clock input/output
89	EFM	I/O	PLL input/output
90	ADPLCK	I/O	ADIP-PLL clock input/output
91	ADIP-DATA	I/O	ADIP-PLL demodulation input/output
92	TEST	I	Test
93	CRCF	O	CRC flag
94	ERFLAG	O	Error flag
95	FON	O	FON signal
96	FOK	O	FOK signal
97	ID3	I	SSB code setting input
98	ID2	I	SSB code setting input
99	ID1	I	SSB code setting input
100	ID0	I	SSB code setting input