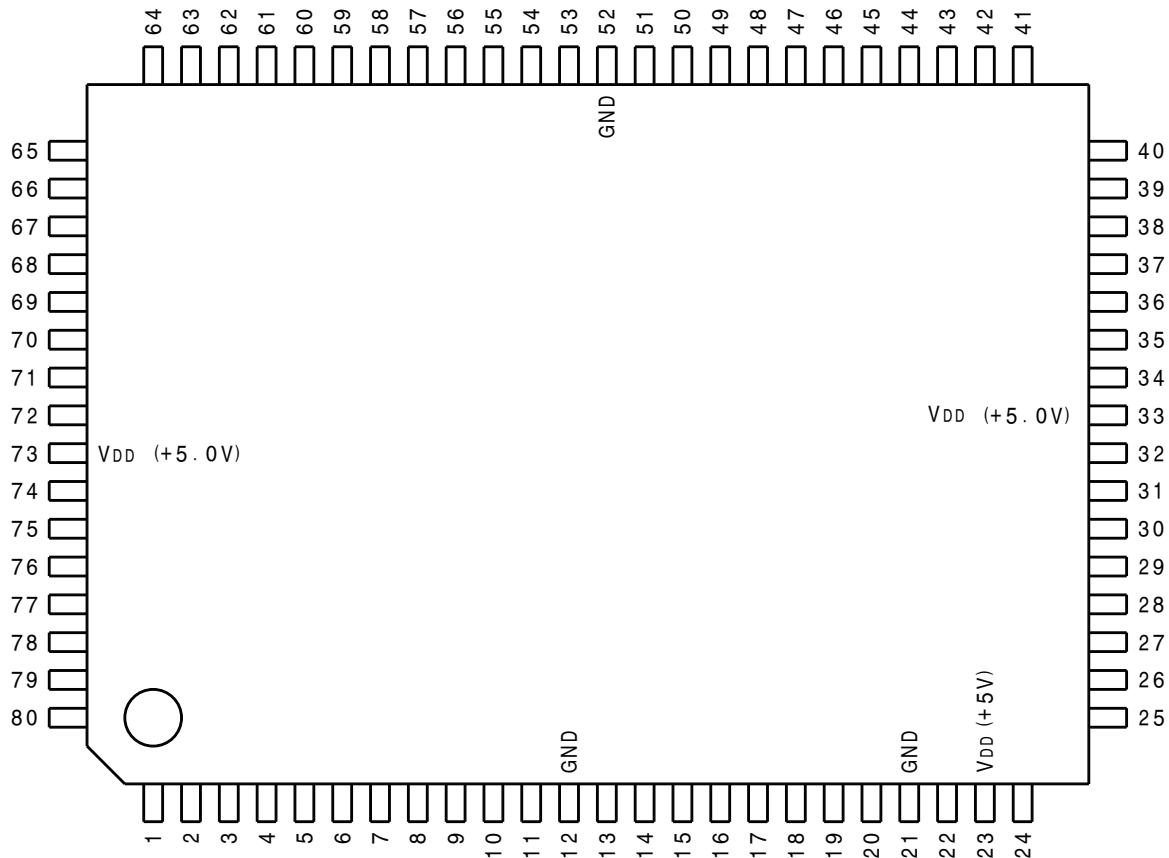
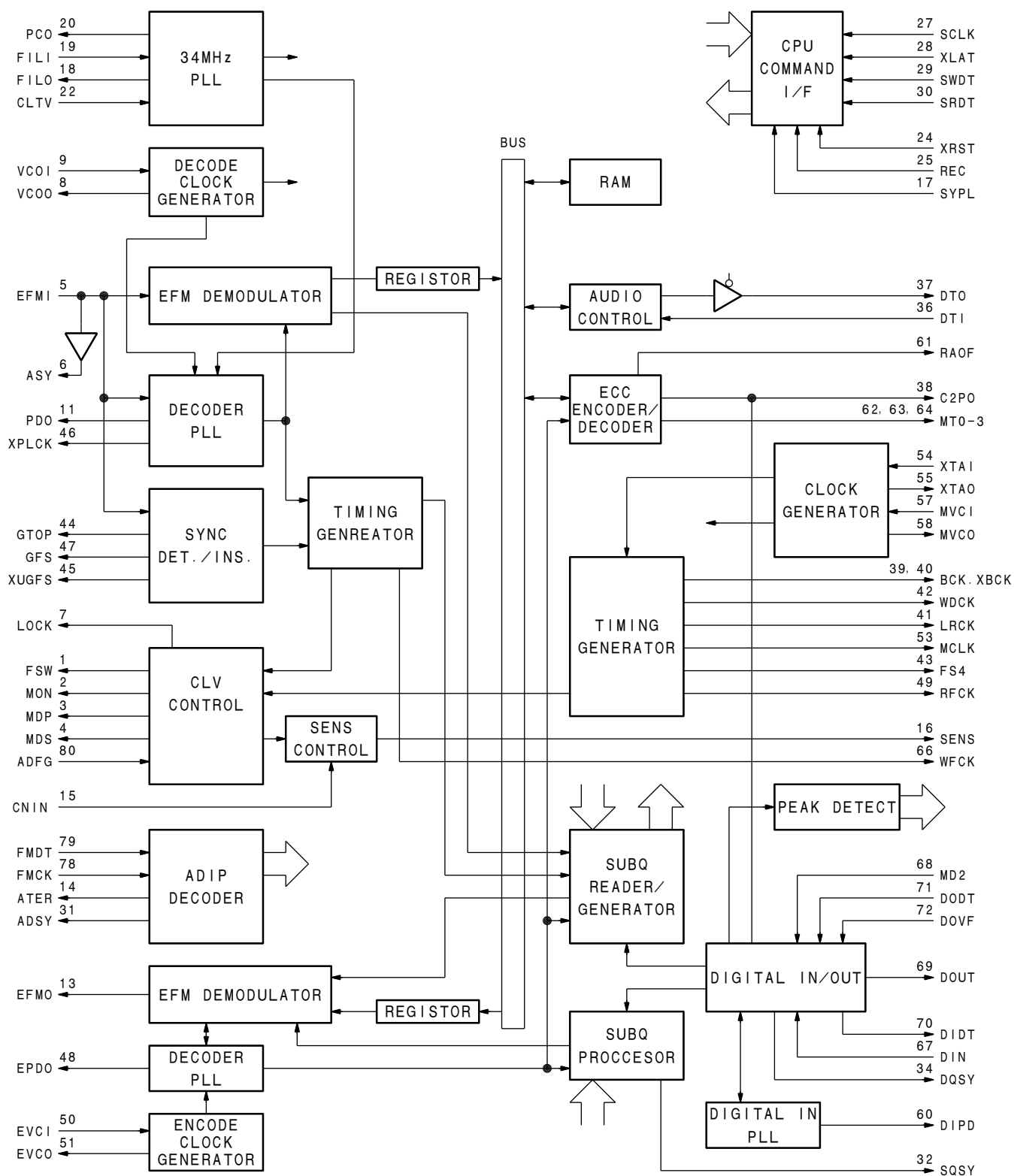

EFM · ACIRC ENCODER/DECODER

-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	FSW	21	-	GND	41	O	LRCK	61	O	RAOF
2	O	MON	22	I	CLTV	42	O	WDCK	62	O	MT3
3	O	MDP	23	-	VDD	43	O	FS4	63	O	MT2
4	O	MDS	24	I	XRST	44	O	GTOP	64	O	MT1
5	I	EFMI	25	I	REC	45	O	XUGFS	65	O	MT0
6	O	ASY	26	I	TEST8	46	O	XPLCK	66	O	WFCK
7	O	LOCK	27	I	SCLK	47	O	GFS	67	I	DIN
8	O	VCOO	28	I	XLAT	48	O	EPDO	68	I	MD2
9	I	VCOI	29	I	SWDT	49	O	RFCK	69	O	DOUT
10	I	TEST1	30	O	SRDT	50	I	EVCI	70	O	DIDT
11	O	PDO	31	O	ADSY	51	O	EVCO	71	I	DODT
12	-	GND	32	O	SQSY	52	-	GND	72	I	DOVF
13	O	EFM0	33	-	VDD	53	O	MCLK	73	-	VDD
14	O	ATER	34	O	DQSY	54	I	XTAI	74	I	TEST3
15	I	CNIN	35	O	TEST7	55	O	XTAO	75	O	TEST4
16	O	SENS	36	I	DTI	56	I	TEST9	76	I	TEST5
17	I	SYPL	37	O	DTO	57	I	MVCI	77	I	TEST6
18	O	FIL0	38	O	C2PO	58	O	MVCO	78	I	FMCK
19	I	FILI	39	O	BCK	59	O	TEST2	79	I	FMDT
20	O	PCO	40	O	XBCK	60	O	DIPD	80	I	ADFG



19	FIL I	PCO	20
22	CLTV	FIL O	18
9	VCO I	VCO O	8
5	EFMI	ASY	6
80	ADFG	PDO	11
78	FMCK	XPLCK	46
79	FMDT	GTOP	44
54	XTA I	GFS	47
57	MVC I	XUGFS	45
		XTA O	55
		MVCO	58
		LOCK	7
		FSW	1
		MON	2
		MDP	3
		MDS	4
		ATER	14
		ADSY	31
		BCK	39
		XBCK	40
		LRCK	41
		WDCK	42
		FS4	43
		MCLK	53
		RFCK	49
50	EVC I	EVC O	51
68	MD2	EPDO	48
71	DODT	EFMO	13
72	DOVF	DOUT	69
67	DIN	DIDT	70
		DQSY	34
		DIPD	60
		SQSY	32
36	DTI	DTO	37
		RAOF	61
		C2PO	38
		MT3	62
		MT2	63
		MT1	64
		MT0	65
27	SCLK	SRDT	30
28	XLAT		
29	SWDT		
17	SYPL		
24	XRST		
25	REC		
15	CNIN	WFCK	66
10	TEST1	SENS	16
74	TEST3	TEST2	59
76	TEST5	TEST4	75
77	TEST6	TEST7	35
26	TEST8		
56	TEST9		

FSW ; SPINDLE MOTOR OUTPUT FILTER SWITCHING OUTPUT
 MON ; SPINDLE MOTOR ON/OFF CONTROL OUTPUT, WHEN "H" : ON
 MDP ; SPINDLE MOTOR SERVO CONTROL
 MDS ; SPINDLE MOTOR SERVO CONTROL
 EFM1 ; EFM INPUT WHEN PLAYBACK MODE
 ASY ; EFM FULL SWING OUTPUT WHEN PLAYBACK MODE
 LOCK ; SPINDLE SERVO (CLV) LOCKED STATE MONITOR, WHEN "H" : LOCKED
 VCO0 ; EFM DECODER, ANALOG PLL OSCILLATION OUTPUT (196Fs=8.6436MHz)
 VCO1 ; EFM DECODER, ANALOG PLL OSCILLATION INPUT
 TEST1 ; TEST PIN (NORMALLY SET TO GROUND)
 PDO ; EFM DECODER, ANALOG PLL PHASE COMPARISON OUTPUT
 EFMO ; EFM OUTPUT WHEN REC MODE
 ATER ; ADIP CRC FLAG OUTPUT, WHEN "H" : ERROR
 CNIN ; TRACK JUMP NUMBER COUNT SIGNAL INPUT
 SENS ; INTERNAL STATUS OUTPUT
 SYPL ; POLARITY SWITCHING INPUT PIN OF SQSY, ADSY, AND DQSY
 FIFO ; MASTER PLL FILTER OUTPUT FOR DIGITAL PLL
 FIL1 ; MASTER PLL FILTER INPUT FOR DIGITAL PLL
 PCO ; MASTER PLL PHASE COMPARISON OUTPUT FOR DIGITAL PLL
 CLTV ; MASTER PLL VCO CONTROL VOLTAGE INPUT FOR DIGITAL PLL
 XRST ; SYSTEM RESET INPUT (ACTIVE LOW)
 REC ; WHEN "L" : DECODER, "H" : ENCODER
 TEST8 ; TEST PIN (NORMALLY SET TO GROUND)
 SCLK ; SERIAL BUS CLOCK INPUT
 XLAT ; SERIAL BUS LATCH INPUT
 SWDT ; SERIAL BUS WRITE DATA INPUT
 SRDT ; SERIAL BUS READ OUT DATA OUTPUT
 ADSY ; ADIP SYNC OUTPUT
 SQSY ; SUBCODE Q SYNC OUTPUT
 DQSY ; SUBCODE Q SYNC (SCOR) OUTPUT OF DIGITAL IN U-BIT CD FORMAT
 TEST7 ; SET TO "OPEN"
 DT1 ; RECORDING AUDIO SIGNAL INPUT
 DT0 ; PLAYBACK AUDIO SIGNAL OUTPUT, (REC MODE; HIGH-IMPEDANCE)
 C2P0 ; SET TO C2P0 WHEN PLAYBACK, D. IN-VFLAG WHEN D. REC, A. REC
 WHEN "0" .
 BCK ; 2.8224MHz OUTPUT (MCLK SYSTEM)
 XBCK ; BCK INVERSION OUTPUT (MCLK SYSTEM)
 LRCK ; 44.1kHz (=Fs) (MCLK SYSTEM)
 WDCK ; 88.2kHz (MCLK SYSTEM)
 FS4 ; 176.4kHz (MCLK SYSTEM)
 GTOP ; WHEN "H" : SYNC GUARD WINDOW OPENS (INPUT EFM SYNC MONITOR OUTPUT)
 XUGFS ; WHEN "L" : UNGUARDED FRAME SYNC (INPUT EFM SYNC MONITOR OUTPUT)
 XPLCK ; EFM DECODER PLL CLOCK OUTPUT (98Fs=4.3218MHz)

GFS ; WHEN "H" : FRAME SYNC OK (INPUT EFM SYNC MONITOR OUTPUT)
 EPDO ; EFM ENCODER EXTERNAL PLL PHASE COMPARISON OUTPUT
 RFCK ; 7.35kHz OUTPUT (MCLK SYSTEM)
 EVC1 ; EFM ENCODER EXTERNAL PLL OSCILLATION INPUT (196Fs=8.6436MHz)
 EVC0 ; EFM ENCODER OUTSIDE PLL OSCILLATION OUTPUT (196Fs=8.6436MHz)
 MCLK ; 22.5792MHz OUTPUT
 XTAI ; CRYSTAL OSCILLATION INPUT (512Fs=22.5792MHz)
 XTAO ; CRYSTAL OSCILLATION OUTPUT (512Fs=22.5792MHz)
 MVC1 ; DIGITAL IN PLL OSCILLATION INPUT (512Fs=22.5792MHz)
 MVCO ; DIGITAL IN PLL OSCILLATION OUTPUT (512Fs=22.5792MHz)
 DIPD ; DIGITAL IN PLL PHASE COMPARISON OUTPUT
 RAOF ; RAM OVERFLOW OUTPUT (DECODER MONITOR OUTPUT)
 MT0-3 ; CORRECTING STATE MONITOR OUTPUT
 WFCK ; 7.35kHz OUTPUT. (SET TO EFM DECODER PLL SYSTEM WHEN
 PLAYBACK, EFM DECODER PLL SYSTEM WHEN RECORDING.)
 DIN ; DIGITAL AUDIO INPUT
 MD2 ; DIGITAL AUDIO OUTPUT ON/OFF ("H" : ON)
 DOUT ; DIGITAL AUDIO OUTPUT
 DIDT ; AUDIO DATA OUTPUT OF DIGITAL AUDIO INPUT
 DODT ; 16-BIT DATA INPUT FOR DIGITAL AUDIO OUTPUT
 DOVF ; VALIDITY FLAG INPUT FOR DIGITAL AUDIO OUTPUT
 TEST9, 3, 5, 6 ; FIXED TO "L"
 TEST2, 4, 7 ; SET TO "OPEN"
 FMCK ; ADIP READ OUT CLOCK INPUT (6.3kHz)
 FMDT ; ADIP DATA INPUT
 ADFG ; ADIP CARRIER SIGNAL INPUT